AMENDED CLAIM SET:

1. (currently amended) A field effect device, comprising:

a crystalline Si body of one conductivity type;

a SiGe layer epitaxially disposed on said Si body;

a Si layer epitaxially disposed on said SiGe layer; ~~and~~

an insulating layer, on top of which said Si body is disposed thereon; and

a source and a drain comprising SiGe in an epitaxial relation with said Si body and connected to each other by said SiGe layer and said Si layer, wherein said source and said drain are formed in recessed source/drain regions of said body, wherein said recessed source/drain regions penetrate all the way down to said insulating layer, said source and said drain having a conductivity type opposite to that of said Si body and each forming a heterojunction and a metallurgical junction with said Si body, wherein said heterojunction coincides with said metallurgical junction with a tolerance of less than about 10nm.

2. (canceled)

3. (canceled)

4. (currently amended) The device of claim ~~3~~ 1, wherein said insulating layer is SiO_2.

5. (original) The device of claim 1, wherein said Si body conductivity is n-type, and wherein a hole device current is confined predominantly in said SiGe layer.

6. (original) The device of claim 5, wherein said hole device current is directed along one of a <100> or a <110> crystallographic direction.

7. (original) The device of claim 1, wherein said Si body conductivity is p-type, and an electron device current is confined predominantly in said Si layer.

8. (original) The device of claim 1, wherein said SiGe layer and said SiGe in said source and said drain are compressively strained.

9. (original) The device of claim 1, wherein said SiGe layer is between about 5nm and 15nm thick.

10. (original) The device of claim 1, wherein said SiGe layer has a Ge concentration which substantially equals a Ge concentration in said SiGe in said source and said drain.

11. (original) The device of claim 10, wherein said Ge concentration in said SiGe layer is between about 15% and 50%.

12. (canceled)

13. (original) The device of claim 1, wherein said device has a top surface plane that lies essentially in one of a (100), (110) or (111) crystallographic plane.

14. (original) The device of claim 1, wherein said source and said drain further comprise an epitaxial Si cap layer disposed on top of said strained SiGe, wherein said Si cap layer is between about 2nm and 30nm thick.

15. - 17. (canceled)

18. (original) The device of claim 1, wherein said Si body conductivity is n-type, and said device is connected in a complementary circuit configuration with an NMOS device.

19. (currently amended) A PMOS field effect device, comprising:

a crystalline Si body ~~of n-type conductivity~~;

a SiGe layer epitaxially disposed on said ~~n-type~~ Si body;

a Si layer epitaxially disposed on said SiGe layer; ~~and~~

an insulating layer, on top of which said Si body is disposed thereon; and

a source and a drain of p-type conductivity comprising SiGe in an epitaxial relation with said ~~n-type~~ Si body and connected to each other by said SiGe layer and said

Si layer, wherein said p-type source and said p-type drain are formed in recessed source/drain regions of said ~~n-type~~ body, wherein said recessed source/drain regions penetrate all the way down to said insulating layer, said source and said drain each forming a heterojunction and a metallurgical junction with said n-type Si body, wherein said heterojunction coincides with said metallurgical junction with a tolerance of less than about 10nm.

20. (canceled)

21. (canceled)

22. (currently amended) The device of claim ~~21~~ 19, wherein said insulating layer is SiO_2.

23. (original) The device of claim 19, wherein said SiGe layer is between about 5nm and 15nm thick.

24. (original) The device of claim 19, wherein said SiGe layer has a Ge concentration of between about 15% and 50%.

25. (original) The device of claim 24, wherein said Ge concentration in SiGe layer substantially equals a Ge concentration in said SiGe in said source and said drain.

26. - 37. (canceled)

38. (currently amended) A processor, comprising:

at least one chip, wherein said chip comprises at least one field effect device, and wherein said at least one field effect device comprise:

a crystalline Si body of one conductivity type;

a SiGe layer epitaxially disposed on said Si body;

a Si layer epitaxially disposed on said SiGe layer; ~~and~~

an insulating layer, on top of which said Si body is disposed thereon; and

a source and a drain comprising SiGe in an epitaxial relation with said Si body and connected to each other by said SiGe layer and said Si layer, wherein said source and said drain are formed in recessed source/drain regions of said body, wherein said recessed source/drain regions penetrate all the way down to said insulating layer, said source and said drain having a conductivity type opposite to that of said Si body and each forming a heterojunction and a metallurgical junction with said Si body, wherein said heterojunction coincides with said metallurgical junction with a tolerance of less than about 10nm.

39. (canceled)